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ROUTER REDUNDANCY SYSTEM AND METHOD

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Pursuant to 35 U.S.C. § 119(a), this application claims the benefit of earlier filing date and right of priority to the Korean Application No. 2002-44323, filed on July 26, 2002, the content of which is hereby incorporated by reference herein in its entirety

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a routing system and, more particularly, to a router redundancy system and method.

Description of the Background Art

[0003] A router is a device for checking a destination address of a packet being transferred through a network and transferring the packet via the most suitable communication path. For duplexing (i.e., to provide data redundancy backup) for an active board (i.e., a first unit), generally, the router includes a standby board (i.e., a second unit) in case of a failure of the active board. Herein after, the terms active board and standby board, are

interchangeably used instead of a first unit or a second unit, respectively.

[0004] The invention, in accordance with one or more embodiments, is disclosed as applicable to an active board and standby board. This application, however, is by way of example. As such, the invention should not be construed as limited to active and standby boards in a routing system. In alternative embodiments, the methods and implementation disclosed here may be applicable to other system components and units that can benefit from data redundancy features.

[0005] The router periodically duplicates/mirrors data stored in a memory of the active board to a memory of the standby board. That is, mirroring or redundancy means are provided for storing the same data in two or more units in order to prevent a data loss due to failure of equipment. Figure 1 illustrates a construction of a router duplexing apparatus in accordance with conventional art, showing a path of mirroring a NVRAM data of an active board to a standard board.

[0006] Memory units 10A and 10B store log information and configuration information (e.g., IP addresses of each router interface, a sub-net mask, an access list). The memory units, generally, include a nonvolatile random access memory (NV RAM). The NV RAM is a memory device for preserving stored data even if power is cut off from an external source.

[0007] As shown in Figure 1, a north bridge 40A of the active board reads data stored in the memory unit 10A (referred to as 'memory data', hereinafter), and transfers the data to a PCI-to-PCI bridge 50A (or an Ethernet controller). Then, the PCI-to-PCI bridge 50A outputs the memory data to the standby board. The memory data outputted from the active board is received by the standby board through a PCI-to-PCI bridge 50B, and a NORTH bridge 40B

reads the memory data received by the PCI-to-PCI bridge 50B and stores it in the standby memory 10B.

[0008] Due to the characteristics of the PCI-to-PCI bridge 50A, a certain time delay occurs when the memory data is transferred from the active board to the standby board. Therefore, as mentioned above, the conventional duplexing apparatus has the following problems.

[0009] For example, time is required for the periodical mirroring operation, and while the mirroring operation is performed, memory access of other elements is limited. In addition, when the memory of the active board is updated, it is preferred that the memory of the standby board is updated simultaneously. In the conventional art, however, because the communication between the active board and the standby board are made through the PCI-to-PCI bridges 50A and 50B (or the Ethernet controller), a real time mirroring is not possibly implemented.

[0010] As such, methods and systems are needed to overcome the shortcoming of the prior art systems.

SUMMARY OF THE INVENTION

[0011] A router apparatus in accordance with one or more embodiments of the invention is provided. In one embodiment, routing information of an active board is mirrored to a standby board in real time, wherein at least one of the active board and the standby board comprises at least one switching unit for transferring the routing information from the active board to the standby board, eliminating use of a PCI-to-PCI board to complete transferring the routing information.

[0012] When the routing information is stored in a first memory of a first switching unit, and the first switching unit transfers the information to the standby

board. A second switching unit receives the routing information from the first switching unit and stores the routing information in a second memory of the standby board.

[0013] The second switching unit prevents signal transmission form the standby board to the second memory, in certain embodiments. When the first memory is loaded, the first switching unit transfers any signal transferred from the active board to the standby board. The second switching unit prevents data from being loaded from the second memory.

[0014] In some embodiments, the active board comprises a first programmable switch and the standby board comprises a second programmable switch. The first and second switching units can be structural equivalents. Alternatively, the first and second switching units may be functional equivalents.

[0015] In accordance with another embodiment, a routing redundancy apparatus comprises an active board for storing routing information in a first memory and for simultaneously transferring the routing information to a standby board by using a first switching unit; and a standby board for receiving the routing information by way a second switching unit and storing it in a second memory.

[0016] While the routing information is stored in the second memory, the second switching unit prevents signal transmission to the second memory, and when the first memory is loaded, the first switching unit prevents signal transmission form the active board to the standby board. In some embodiments, the second switching unit of standby board prevents the second memory from being loaded.

[0017] In accordance with yet another embodiment, a data redundancy system comprises a first switching unit; a second switching unit; an active board

comprising a first memory for storing routing information; and a standby board comprising a second memory for storing routing information transferred from the active board. In certain embodiments, the active board further comprises the first switching unit and the standby board further comprises the second switching unit. The routing information is transferred from the active board to the standby board via the first and second switching unit. Accordingly, the first switching unit causes the routing information stored in the first memory to be transferred to the second memory via the second switching unit.

[0018] In one or more embodiments, the first switching unit comprises at least one multiplexer; and at least one tristate output buffer in communication with the at least one multiplexer; wherein the first switching unit is configured to connect to a plurality of external devices to route a signal inputted from a first device to a second device, according to control information. The multiplexer is a 2:1 multiplexer comprising two input terminals; one output terminal; and one control terminal responsive to a select signal, for example.

[0019] When a select signal is in a first state, the at least one multiplexer outputs a first signal, and when the select signal is in a second state, the at least one multiplexer outputs a second signal. In one embodiment, the at least one tristate output buffer is connected to the output terminal of the at least one multiplexer, wherein when the select signal is equal to a first value, the tristate output buffer is in an output-enable state, and when the select signal is equal to a second value, the tristate output buffer is in an output-disable state.

[0020] In accordance with one embodiment, a method of providing data redundancy in a routing system having a first switching unit, a second switching unit, an active board comprising a first memory, and a standby board comprising a

second memory, comprises loading the first memory with routing information received by the active board; transferring the routing information from the first board to the standby board via the first switching unit in communication with the second switching unit; and loading the second memory with the routing information. In some embodiments, when a select signal is in a first state, the at least one multiplexer outputs a first signal, and when the select signal is in a second state, the at least one multiplexer outputs a second signal.

[0021] These and other embodiments of the present invention will also become readily apparent to those skilled in the art from the following detailed description of the embodiments having reference to the attached figures, the invention not being limited to any particular embodiments disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0023] Figure 1 illustrates a related art routing duplexing apparatus;

[0024] Figure 2 illustrates a routing duplexing apparatus in accordance with one embodiment of the present invention;

[0025] Figure 3 illustrates a structure of a device switch (GDX) in accordance with one embodiment;

[0026] Figure 4 shows a routing information transfer path according to a write command in one embodiment; and

[0027] Figure 5 shows a routing information transfer path, according to a read command.

[0028] Features, elements, and aspects of the invention that are referenced by the same numerals in different figures represent the same, equivalent, or similar features, elements, or aspects in accordance with one or more embodiments of the system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] Data switching and redundant information management systems and corresponding methods, according to one or more embodiments of the invention are provided. In a data switching method and system, a router sets a communication path on the basis of a memory data of a standby board and transfers data through the path. In the present invention, a real time mirroring operation is performed on the memory data so as for the router to set the most suitable communication path.

[0030] A router duplexing apparatus of the present invention is featured in that routing information of an active board is mirrored to a standby board in real time by using a plurality of switching units. The switching units are respectively provided both in the active board and the standby board.

[0031] Referring to Figure 2, the router duplexing apparatus of the present invention comprises switching units 170A and 170B, in one or more embodiments. The router duplexing apparatus comprises an active board for storing routing information in its memory 110A and transferring the information to a

standby board by using general device switches GDX 170A, and a standby board for receiving the routing information by using a GDX 170B and storing it in its memory 110B.

[0032] The GDXs 170A and 170B are programmable switches for various circuits or communication equipments. Said programmable switches, in one embodiment comprise, for example, 5 multiplexers (m1~m5) and tristate output buffers (b1~b5). The GDX is connected in four sides to external devices that can freely route a signal inputted from each device according to a user's request.

[0033] Referring to Figure 3, the multiplexers (m1~m5) provided in the GDX are 2:1 multiplexers each having two input terminals m0 and m1, one output terminal and one control terminal (select terminal), for example. When the select signal is '1', the multiplexers m1~m5 output a signal m0, and when the select signal '0', the multiplexers m1~m5 output a signal m1.

[0034] In the GDX, the five tristate output buffers b1~b5 are respectively positioned at the output terminals of the multiplexers m1~m5, and respectively have an input terminal, an output terminal and a control terminal (oe). When the signal oe is '1', the tristate output buffers b1~b5 are in an output-enable state, while when the signal oe is '0', the tristate output buffers b1~b5 are in an output-disable state, for example.

[0035] The GDX 170A comprises a multiplexer m1 for selectively outputting output signals (nb_(address, oe, we, cs)) of the NORTH bridge 140A or output signals (mr_(address, oe, we, cs)) of the GDX 170B according to a signal sel1; a buffer b1 for determining whether to output the output signal of the multiplexer m1 to the memory 110A according to a signal oe1; a multiplexer m2 for

receiving output signals (nb_(address, oe, we, cs)) of the NORTH bridge 140A; a buffer b2 for determining whether to output the output signal of the multiplexer m2 to the GDX 170B according to a signal oe2; a multiplexer m3 for receiving a data signal (nv_data) of the memory 10A; a buffer b3 for determining whether to output the output signal of the multiplexer m3 to the NORTH bridge 140A according to a signal oe3; a multiplexer m4 for selectively outputting an output signal (nb_data) of the NORTH bridge 140A and an output signal (mr_data) of the GDX 170B according to a signal sel2; a buffer b4 for determining whether to output the output signal of the multiplexer m4 to the memory 110A according to a signal oe4; a multiplexer m5 for receiving the output signal (nb_data) of the NORTH bridge 140A; and a buffer b5 for determining whether to the output signal of the multiplexer m5 to the GDX 170B according to a signal oe5.

[0036] In one embodiment, the GDX 170B has, for example, the same construction and operation as the GDX 170A. The router duplexing apparatus in accordance with the present invention will now be described in detail. First, each programmable logic device (PLD) 160A and 160B checks a state of the board to which itself belongs, and sets one main board as an active board and the other as a standby board according to the check result. If the board to which the PLD 60A belongs is determined as an active board, the PLD 60A extracts control signals (cs/, oe/ and we/) for the memory 110A from the memory bus between the north bridge 140A and the synchronous dynamic random access memory (SDRAM) 130A.

[0037] If the extracted control signals (cs/, oe/ and we/) are a write command signal, the PLDs 160A and 160B control the GDXs 170A and 170B to set control signals oe1~oe5 and sel1~sel2 for the multiplexers m1~m5 and the

tristate output buffers b1~b5 as shown in below Table 1:

[Table 1]

	GDX (170A)	GDX (170B)
oe1	1	1
oe2	1	0
oe3	0	0
oe4	1	1
oe5	1	0
sel1	0	1
sel2	0	1
oe/	H	H
we/	L	L
cs/	L	L

[0038] Figure 4 shows a routing information transfer path according to a write command. If the control signals (cs/, oe/ and we/) extracted from the memory bus indicate a write command signal, a signal transfer path is set in the GDX 170A as shown in Figure 4, through which routing information (nb_(address, oe, we, cs) & nb_data) of the north bridge 140A is transferred to the memory 110A and simultaneously to the standby board.

[0039] For example, the routing information (nb_(address, oe, we, cs) & nb_data) transferred to the standby board is stored in the memory 110B through the GDX 170B. At this time, the GDX 170B interrupts a signal, if any, transmitted from the north bridge 140B to the memory 110B. Meanwhile, after the active board and the standby board are determined, the control signals (cs/, oe/ and we/) extracted form the memory bus are read command signals, the PLDs 60A and 60B controls the GDXs 170A and 170B to set the control signals (oe1~oe5, sel1~sel2) for the multiplexers m1~m5 and the tristate output buffers b1~b5.

[Table 2]

	GDX (170A)	GDX (170B)
oe1	1	0
oe2	0	0
oe3	1	0
oe4	0	0
oe5	0	0
sel1	0	X
sel2	X	X
oe/	L	L
we/	H	H
cs/	L	L

(X : Don't care)

[0040] Figure 5 shows a routing information transfer path according to a read command. If the control signals (cs/, oe/ and we/) extracted from the memory bus indicate a read command signal, a signal transfer path is set in the GDX 170A as shown in Figure 5 and the routing information (nb_(address, oe, we, cs) & nb_data) of the active board is not transferred to the standby board. Also, the read command signal outputted from the north bridge 140B is not transmitted to the memory 110B.

[0041] In one embodiment, when the router reads the memory of the active board, the signal paths in the GDX 170A and the GDX 170B are set as shown in Figure 5. Accordingly, data of the memory 110A and the memory 110B are not simultaneously outputted, preventing data collision. As so far described, the router duplexing apparatus of the present invention by substituting the conventionally used PCI bridge (or the Ethernet protocol) with a programmable switch provides the following advantages.

[0042] A substantially real time mirroring is accomplished on routing information (or the memory data) of the active board and the signal transfer path in the router is simplified. In addition, when the duplex switching occurs, a routing path is set on the basis of the latest routing information, enhancing a reliability of the router duplexing apparatus.

[0043] The embodiments described above are to be considered in all aspects as illustrative only and not restrictive in any manner. Thus, other exemplary embodiments, system architectures, platforms, and implementations that can support various aspects of the invention may be utilized without departing from the essential characteristics described herein. These and various other adaptations and combinations of features of the embodiments disclosed are within the scope of the invention. The invention is defined by the claims and their full scope of equivalents.